

LCFC NM-D521

S360 Lucienne M/B Schematics Document

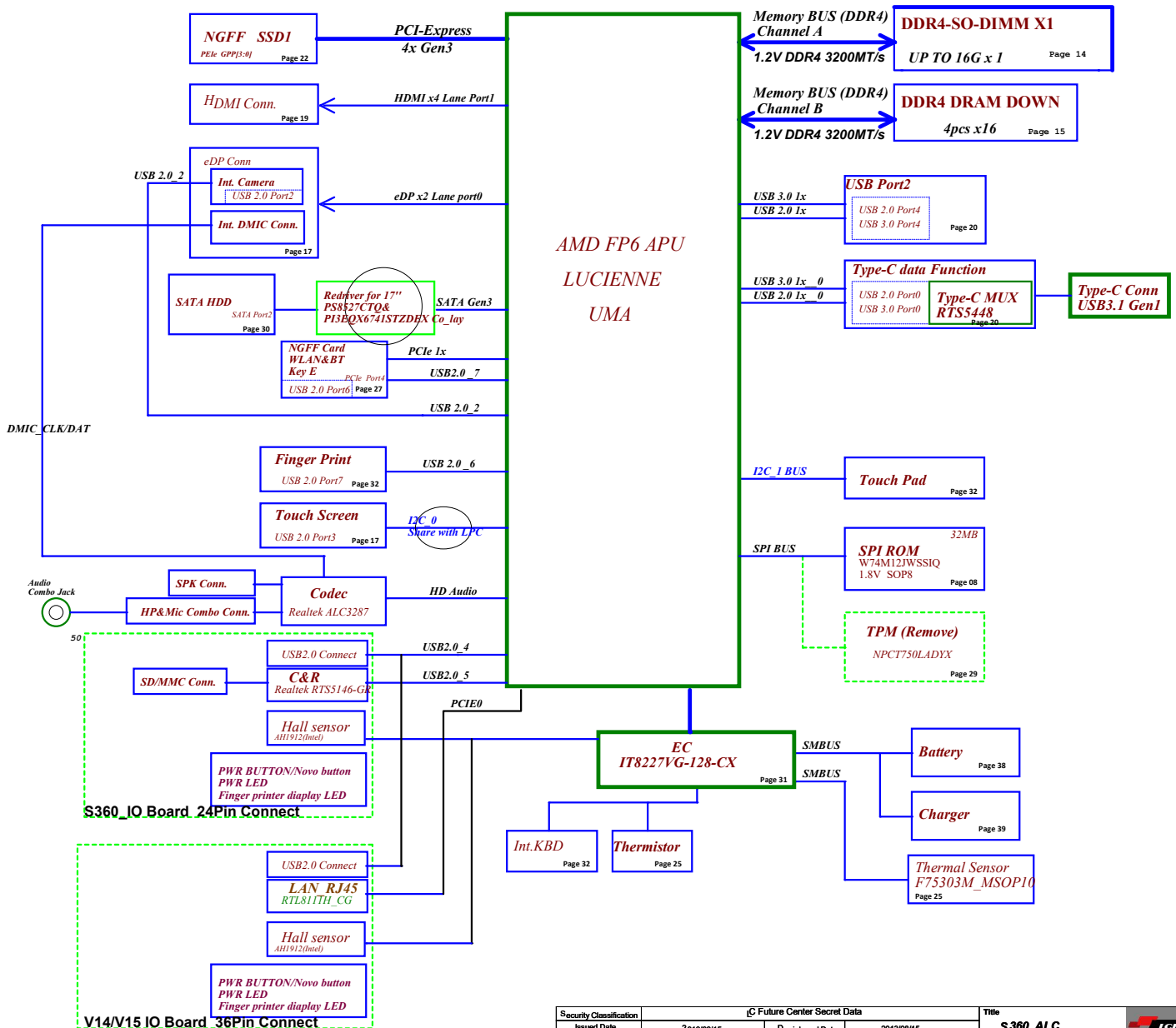
AMD FP6 Lucienne with DDR4

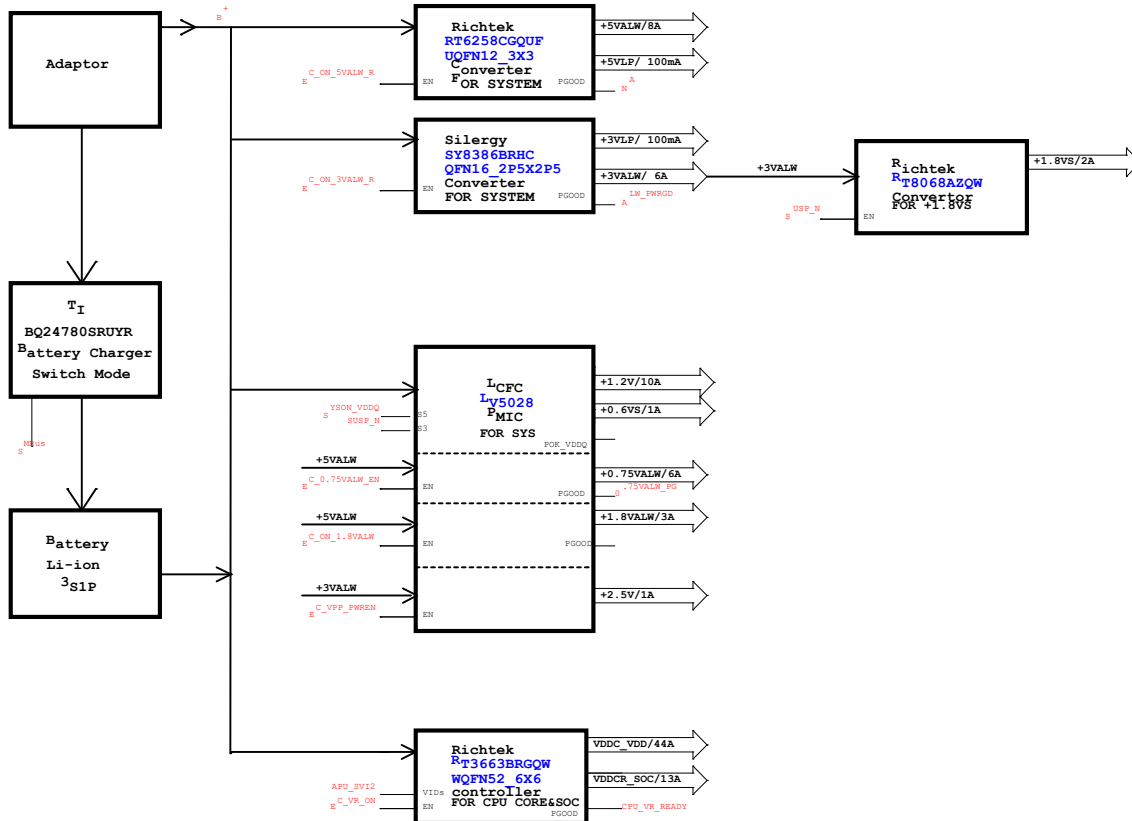
2020-12-01

REV: 1.0

Security Classification	L Future Center Secret Data			Title	S60 ALC	
Issued Date	21/02/27	Revised Date	2020/02/27	Document Number	S60 Lucienne	
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					110	0

S360 Lucienne M/B Schematics





Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane State	B+ +3VL +5VL	+3VALW +5VALW 1.8VALW +0.75VALW		+1.2V +2.5V_DDR	+5VB +3VB +1.8VB +0.75VB 0.6VB +VDDC_VDD +VDDCR_SOC	
S0	O	O		O	O	O
S0Ix						
S3	O	O		O	X	X
S3 Battery only	O	O		O	X	X
S5 S4 AC Only	O	O		X	X	X
S5 S4 Battery only	O	X		X	X	X
S5 S4 AC & Battery don't exist	X	X		X	X	X

HSIO Matrix

HSIO PORT		Function	
USB2.0	0	Type-C USB2.0 Port 0	Type-c Port
	1	USB3.0_P1	
	2	Camera	
	3	Touch_Screen	
	4	USB2.0 Port(For DB USB2.0)	
	5	Cardread	
	6	FingerPrint	
	7	BT	
USB3.0	0	Type-C USB3.0 Port 0	USB3.0 Port
	1	USB3.0_P1	
	4	NC	
	5	NC	
Display	0	eDP 2*1Lane	Follow AT Define ok 0610
	1	HDMI	
	2	NC	
	3	NC	
PCIE/ SATA	PCIE0	LAN	
	PCIE1	WLAN	
	PCIE2/SATA0	SATA HDD	
	PCIE3/SATA1	N/A	
	PCIE4	N/A	
	PCIE5	N/A	
	PCIE6	N/A	
	PCIE7	N/A	
	PCIE8/SATA2	SSD	
	PCIE9/SATA3		
	PCIE10		
	PCIE11		

SMBUS Control Table OK

Source Slave	EC IT9227C				PCH			
	EC_SMB_0 +3VS	EC_SMB_1 +3VL_EC	EC_SMB_3 +3VL_EC	EC_SMB_4 +3VL_EC	I2C0 1.8VB/3.3VB 1.8VB/3.3VB	I2C1 1.8VB/3.3VB	I2C2/SMBUS 1.8VB/3.3VB	
DGPU								
Memory Down	X	X	X	X	X	X	X	X
SODIMM							V 3VS	
BATT	X	V +3VL_EC	X	X	X	X	X	X
Charger	X	V +3VL_EC	X	X	X	X	X	X
WLAN	X	X	X	X	X	X	X	X
PMIC	X	X	V +3VL_EC	X	X	X	X	X
	X	X	X	X	X	X	X	X
Thermal Sensor	V +3VS	X	X	X	X	X	X	X
LPC45T	X	X	X	X	V +3VS CPD	X	X	X
TP	X	X	X	X	X	V 3VS	X	X
	X	X	X	X	X	X	X	X
	X	X	X	X	X	X	X	X

EC SMBus0 address

Device	Address
DGPU	
Thermal Sensor(NCT7710W)	
Thermal Sensor(NCT7719W)	1001_101xb
TOF	

PCH SML0 address

Device	Address
Re-Timer	T BD

PD I2C3 address

Device	Address
Re-Timer	T BD

EC SMBus1 address

Device	Address
Smart Battery	0 x16
Charger	0 x12

PCH SML1 address

Device	Address
PD	T BD

EC SMBus3 address

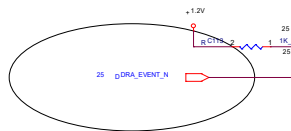
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IMVPS	
PMIC	0 x34

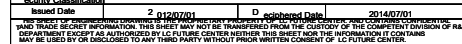
PCH ISH I2C0 address

Device	Address
TOF	
Accelerometer(MB)	0 01 1000b
Accelerometer(DB)	0 01 1001b
Light Sensor	1 000 100xb

EC SMBus4 address

Device	Address
PD	T BD





STRAP PINS

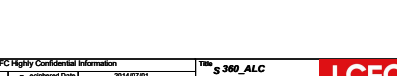
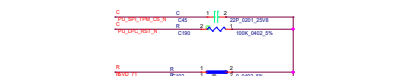
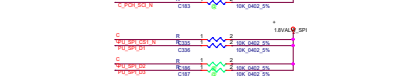
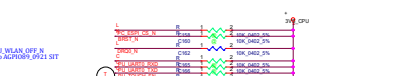
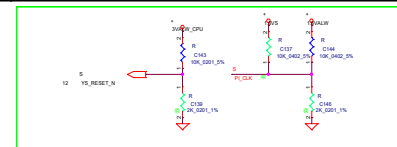
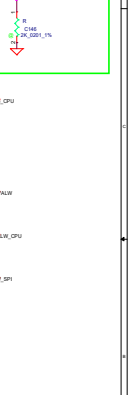
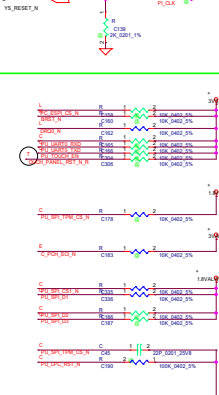
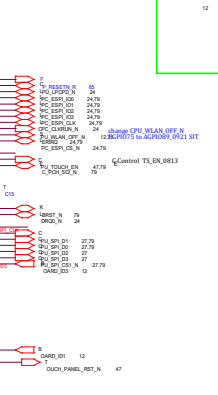
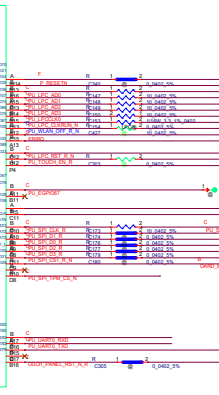
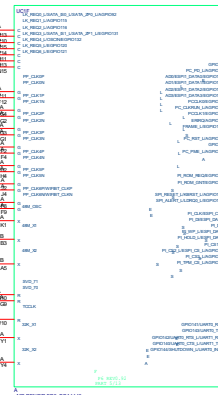
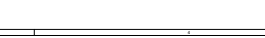
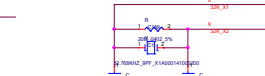
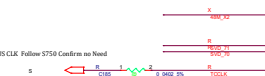
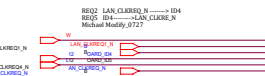
SYS RESET#

PCH_SPI_CLK

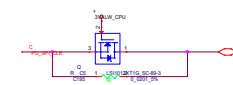
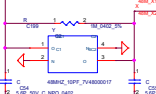
SYS_RESET#

1:USE 48MHZ CRYSTAL CLOCK AND
GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT)
0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND
GENERATE INTERNAL CLOCKS ONLY

1:NORMAL RESET MODE (DEFAULT)
0:SHORT RESET MODE



48MHz/10pF Crystal





V14V15
LAN

WLAN

HDD

SSD

LAN
WLAN
HDD

SSD

TYPE C 1

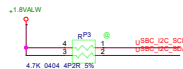
TYPE A charge function

S360

Note: RC347/348 Can't modify 08

Pin 21 Finger print

Pin 27 BT



OC1 Type-C
OC2 USB30

VT change RC341 Stuff to unstuff 1202

VT change RC342 Pull up to RC341 PIN1 to PIN2

VT change RC342 Pull up to RC341 PIN1 to PIN2

VT change RC342 Pull up to RC341 PIN1 to PIN2

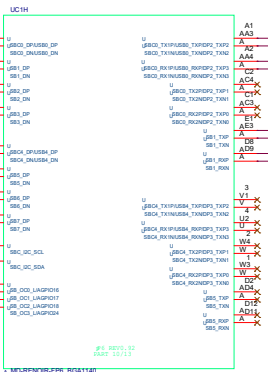
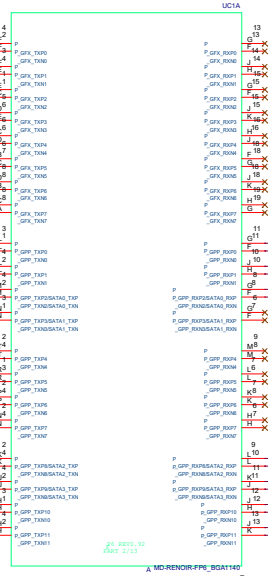
VT change RC342 Pull up to RC341 PIN1 to PIN2

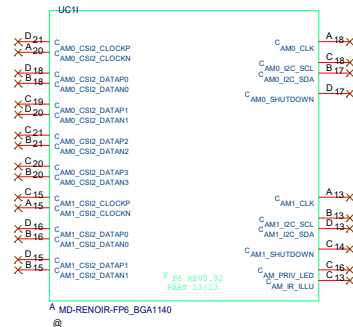
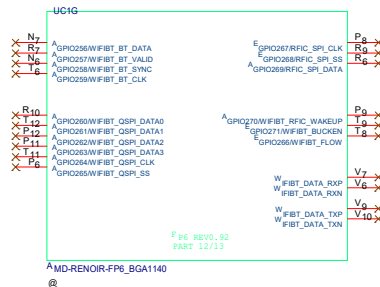
VT change RC342 Pull up to RC341 PIN1 to PIN2

VT change RC342 Pull up to RC341 PIN1 to PIN2

VT change RC342 Pull up to RC341 PIN1 to PIN2

VT change RC342 Pull up to RC341 PIN1 to PIN2





Security Classification		LCFC Highly Confidential Information		Title		S360_ALC		LCFC	
Issued Date		2012/07/01		Deciphered Date		2014/07/01			
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Date		F		Sheet		1.5		9.4 110	



UC1K

A00	05,010	05,001	05,001
A01	05,011	05,002	05,002
A02	05,012	05,003	05,003
A03	05,013	05,004	05,004
A04	05,014	05,005	05,005
A05	05,015	05,006	05,006
A06	05,016	05,007	05,007
A07	05,017	05,008	05,008
A08	05,018	05,009	05,009
A09	05,019	05,010	05,010
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A11	05,021	05,012	05,012
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A15	05,025	05,016	05,016
A16	05,026	05,017	05,017
A17	05,027	05,018	05,018
A18	05,028	05,019	05,019
A19	05,029	05,020	05,020
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A27	05,037	05,028	05,028
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A32	05,042	05,033	05,033
A33	05,043	05,034	05,034
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A43	05,053	05,044	05,044
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A65	05,075	05,066	05,066
A66	05,076	05,067	05,067
A67	05,077	05,068	05,068
A68	05,078	05,069	05,069
A69	05,079	05,070	05,070
A70	05,080	05,071	05,071
A71	05,081	05,072	05,072
A72	05,082	05,073	05,073
A73	05,083	05,074	05,074
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A75	05,085	05,076	05,076
A76	05,086	05,077	05,077
A77	05,087	05,078	05,078
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A100	05,110	05,101	05,101
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A108	05,118	05,109	05,109
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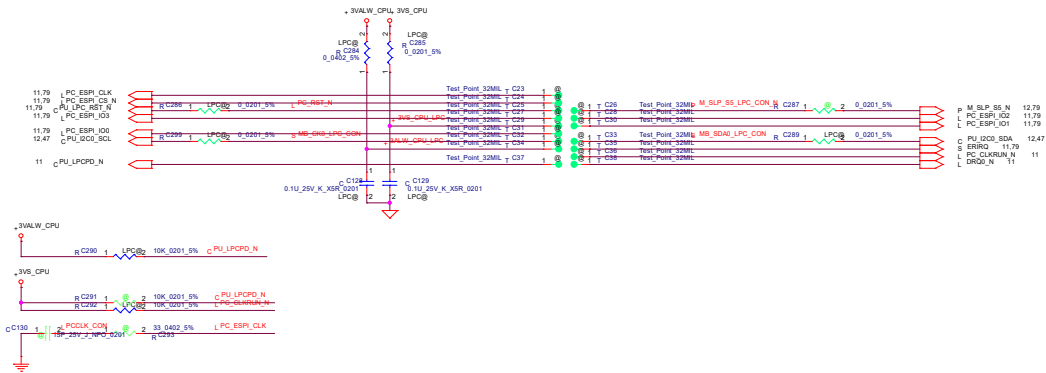
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PART 7/13
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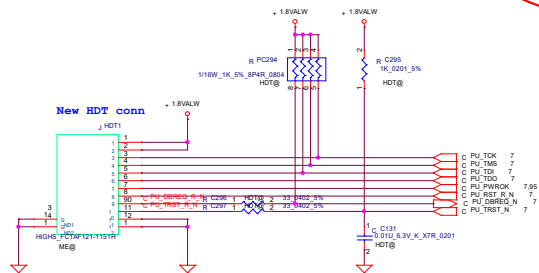
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A134	05,366	05,325	05,325
A135	05,367	05,326	05,326
A136	05,368	05,327	05,327
A137	05,369	05,328	05,328
A138	05,370	05,329	05,329
A139	05,371	05,330	05,330
A140	05,372	05,331	05,331
A141	05,373	05,332	05,332
A142	05,374	05,333	05,333
A143	05,375	05,334	05,334
A144	05,376	05,335	05,335
A145	05,377	05,336	05,336
A146	05,378	05,337	05,337
A147	05,379	05,338	05,338
A148	05,380	05,339	05,339
A149	05,381	05,340	05,340
A150	05,382	05,341	05,341
A151	05,383	05,342	05,342
A152	05,384	05,343	05,343
A153	05,385	05,344	05,344
A154	05,386	05,345	05,345
A155	05,387	05,346	05,346
A156	05,388	05,347	05,347
A157	05,389	05,348	05,348
A158	05,390	05,349	05,349
A159	05,391	05,350	05,350
A160	05,392	05,351	05,351
A161	05,393	05,352	05,352
A162	05,394	05,353	05,353
A163	05,395	05,354	05,354
A164	05,396	05,355	05,355
A165	05,397	05,356	05,356
A166	05,398	05,357	05,357
A167	05,399	05,358	05,358
A168	05,400	05,359	05,359
A169	05,401	05,360	05,360
A170	05,402	05,361	05,361
A171	05,403	05,362	05,362
A172	05,40		

LPC ROM EMULATOR HEADER



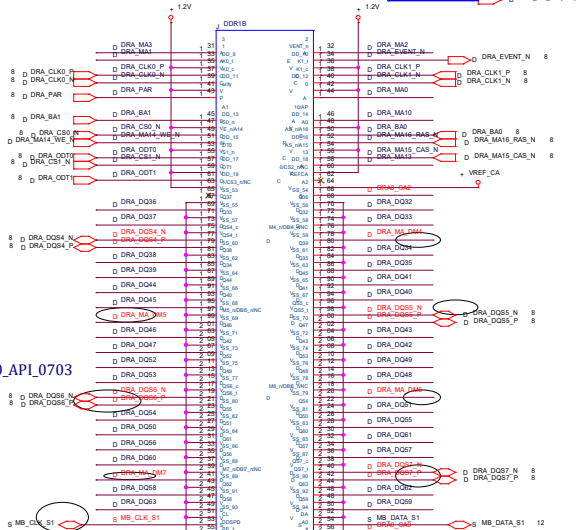
HDT Debug Header



注意下这句话

RC3152 RC3153 should be put on APU side to reduce stub when MP

 DRA_DQ[0..63]	 D	DRA_DQ[0..63]	8
 DRA_MA[0..13]	 D	DRA_MA[0..13]	8
 DRA_MA_DM[0..7]	 D	DRA_MA_DM[0..7]	

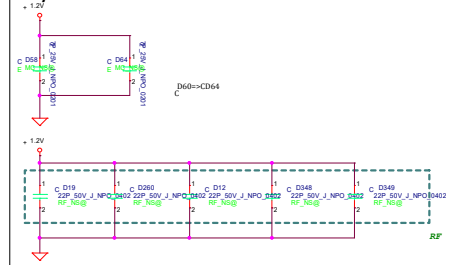


Swap Table

Pin	Net Name
P000	D00A_D00B
P001	D00A_D00B
P002	D00A_D00B
P003	D00A_D003
P004	D00A_D004
P005	D00A_D005
P006	D00A_D006
P007	D00A_D007
P008	D00A_D008
P009	D00A_D009
P010	D00A_D010
P011	D00A_D011
P012	D00A_D012
P013	D00A_D013
P014	D00A_D014
P015	D00A_D015
P016	D00A_D016
P017	D00A_D017
P018	D00A_D018
P019	D00A_D019
P020	D00A_D020
P021	D00A_D021
P022	D00A_D022
P023	D00A_D023
P024	D00A_D024
P025	D00A_D025
P026	D00A_D026
P027	D00A_D027
P028	D00A_D028
P029	D00A_D029
P030	D00A_D030
P031	D00A_D031
P032	D00A_D032
P033	D00A_D033
P034	D00A_D034
P035	D00A_D035
P036	D00A_D036
P037	D00A_D037
P038	D00A_D038
P039	D00A_D039
P040	D00A_D040
P041	D00A_D041
P042	D00A_D042
P043	D00A_D043
P044	D00A_D044
P045	D00A_D045
P046	D00A_D046
P047	D00A_D047
P048	D00A_D048
P049	D00A_D049
P050	D00A_D050
P051	D00A_D051
P052	D00A_D052
P053	D00A_D053
P054	D00A_D054
P055	D00A_D055
P056	D00A_D056
P057	D00A_D057
P058	D00A_D058
P059	D00A_D059
P060	D00A_D060
P061	D00A_D061
P062	D00A_D062
P063	D00A_D063
P064	D00A_D064
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P069	D00A_D069
P070	D00A_D070
P071	D00A_D071
P072	D00A_D072
P073	D00A_D073
P074	D00A_D074
P075	D00A_D075
P076	D00A_D076
P077	D00A_D077
P078	D00A_D078
P079	D00A_D079
P080	D00A_D080
P081	D00A_D081
P082	D00A_D082
P083	D00A_D083
P084	D00A_D084
P085	D00A_D085
P086	D00A_D086
P087	D00A_D087
P088	D00A_D088
P089	D00A_D089
P090	D00A_D090
P091	D00A_D091
P092	D00A_D092
P093	D00A_D093
P094	D00A_D094
P095	D00A_D095
P096	D00A_D096
P097	D00A_D097
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P105	D00A_D105
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P113	D00A_D113
P114	D00A_D114
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P117	D00A_D117
P118	D00A_D118
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P120	D00A_D120
P121	D00A_D121
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P123	D00A_D123
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P130	D00A_D130
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P132	D00A_D132
P133	D00A_D133
P134	D00A_D134
P135	D00A_D135
P136	D00A_D136
P137	D00A_D137
P138	D00A_D138
P139	D00A_D139
P140	D00A_D140
P141	D00A_D141
P142	D00A_D142
P143	D00A_D143
P144	D00A_D144
P145	D00A_D145
P146	D00A_D146
P147	D00A_D147
P148	D00A_D148
P149	D00A_D149
P150	D00A_D150
P151	D00A_D151
P152	D00A_D152
P153	D00A_D153
P154	D00A_D154
P155	D00A_D155
P156	D00A_D156
P157	D00A_D157
P158	D00A_D158
P159	D00A_D159
P160	D00A_D160
P161	D00A_D161
P162	D00A_D162

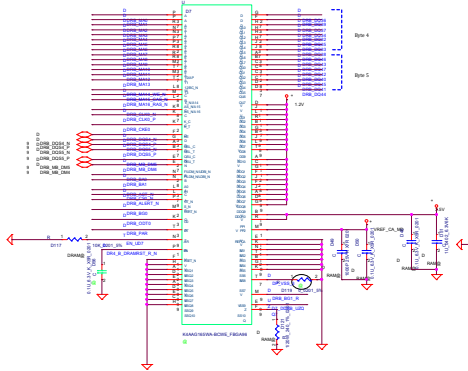
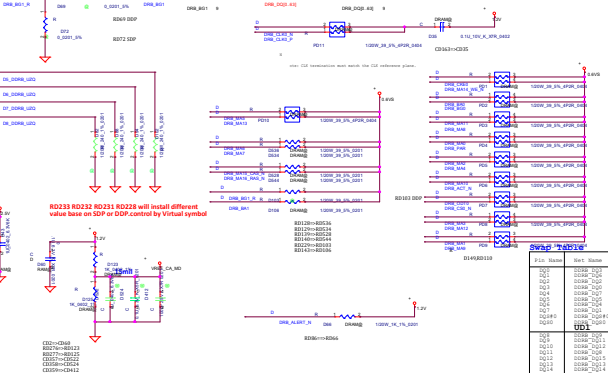
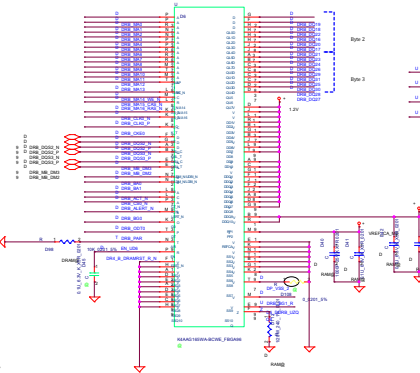
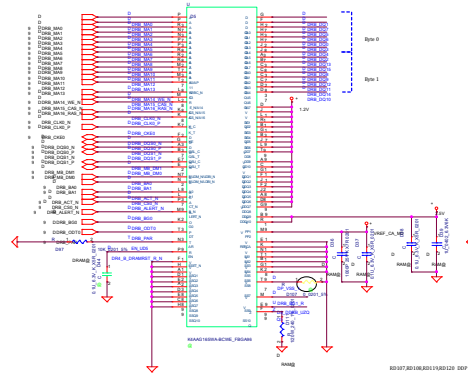


Layout Note: Place near JDDR1



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S 360 Lucienne



Check timing sequence in SDV phase.

SPI ROM

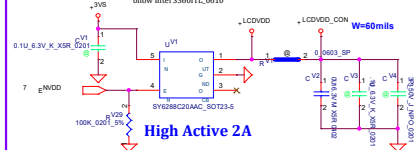
Used RPMC BIOS ROM



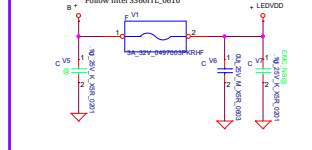
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Issued Date		2018/8/9		Expiry Date		2018/8/9		Document Number	
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Date		C		SI ROM		Sheet		27 of 110	

LCD EDP Display

LCD Power Circuit

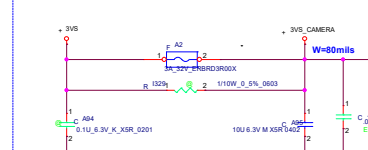


LED Power

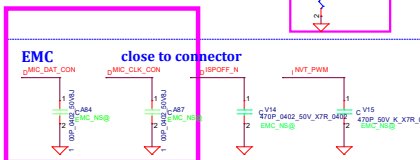
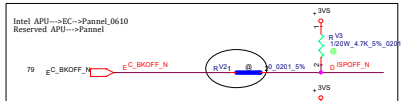
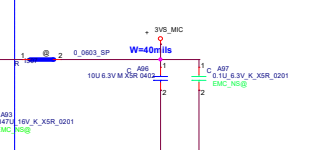


DMIC BOARD POWER

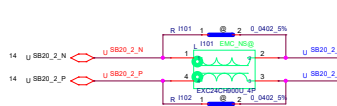
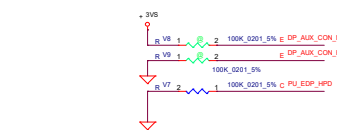
Camera



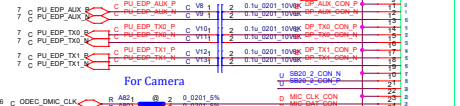
DMIC



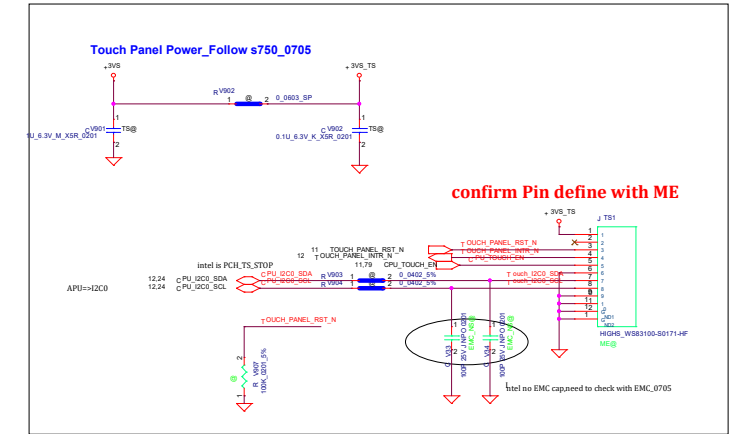
EMC

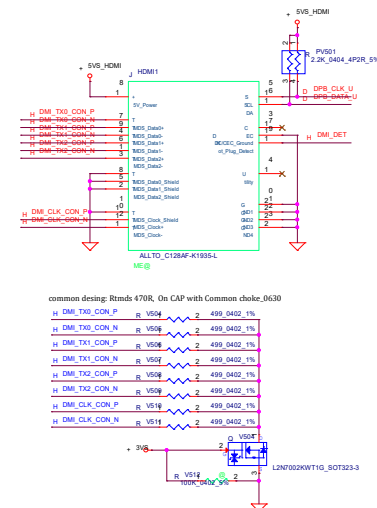
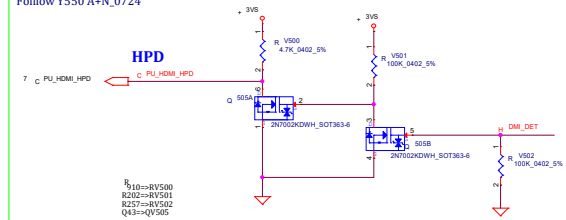
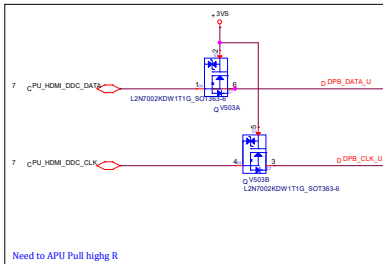


For DMIC



Touch Screen

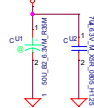


[illegible]

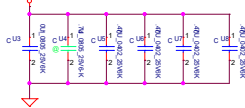
common desing: Rtmids 470R, On CAP with Common choke_0630

[illegible]

+5VALW



VBUS_P0

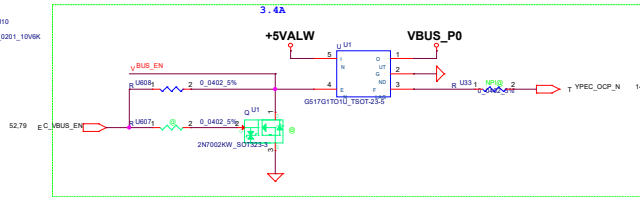


+5VALW



Change R134 0R to 10K,
ADD IC control Power output_SIT 0921

3.4A



Rp configuration
Rp:3A (now)

	M1	M0	Note
Rp:900mA	0	1	RU14/RU15 mount
Rp:1.5A	1	0	RU13/RU16 mount
Rp:3.0A	1	1	RU13/RU15 mount

For C_VBUS
power switch enable pin

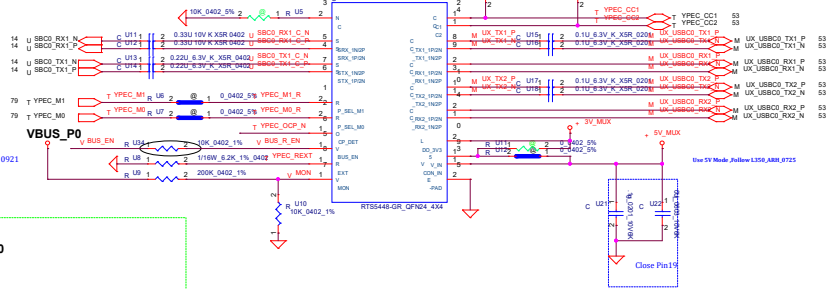
Power switch enable pin	Note
Low Active	RU17 mount
High Active	RU18 mount

PU AT CPU side 0725

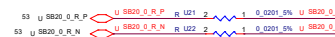
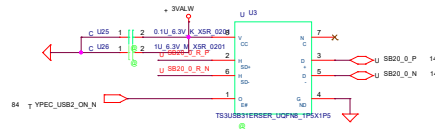
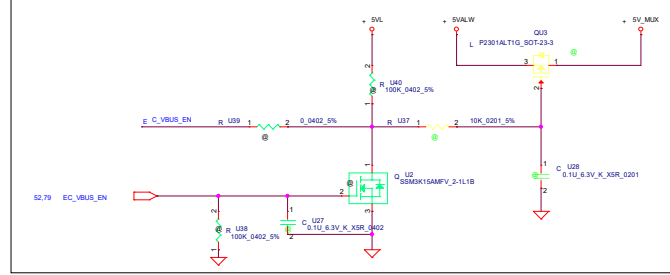
For C_VBUS
power switch OCP pin

Power switch OCP pin	Note
Low Active	RU19 mount
High Active	RU20 mount

%VT change RU19 unstuff to stuff for solve DC SS to 50 U DISK LOSS, L204



add reserved MUX power control_0926



Security Classification: LCFC Highly Confidential Information

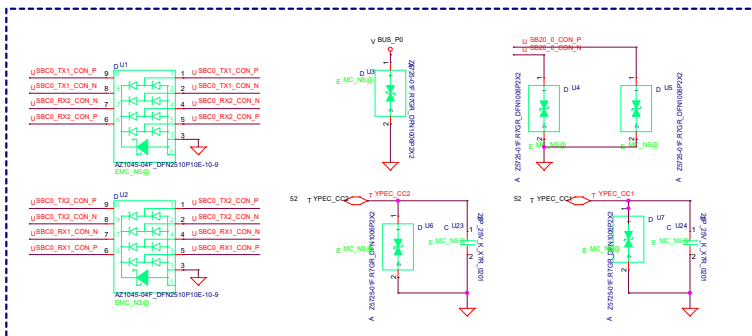
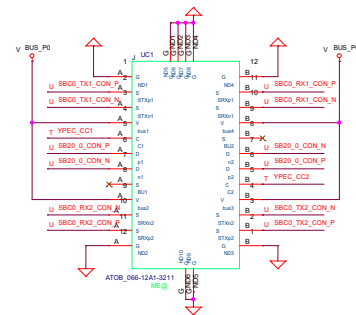
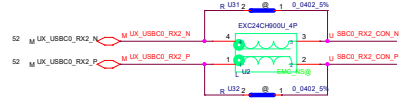
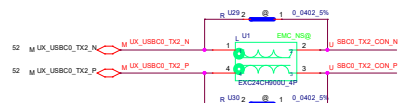
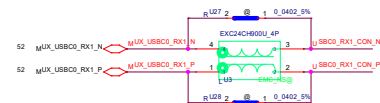
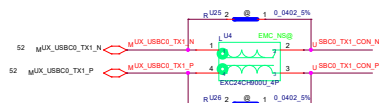
Issued Date: 2 012/07/01

Document Number: T YPEC MUX Porta

Page: 3

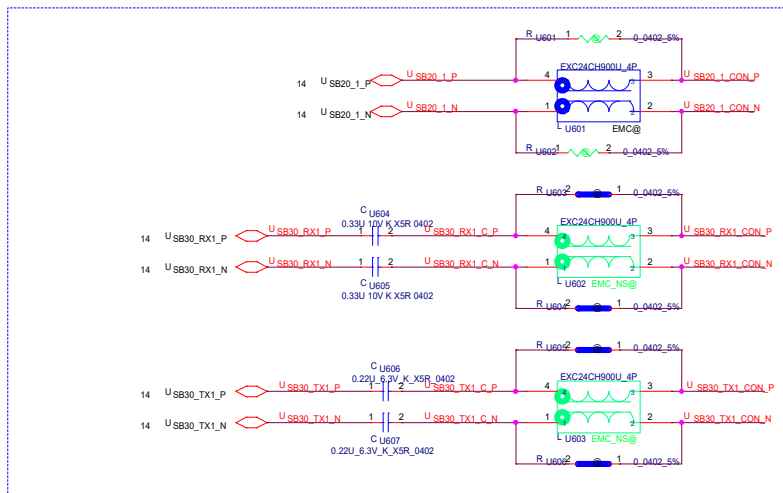
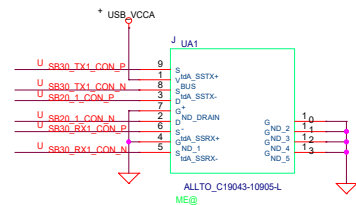
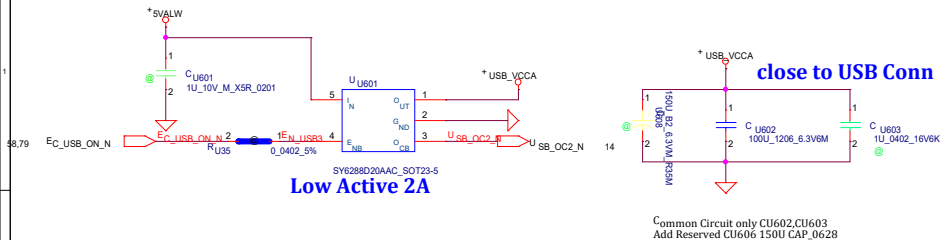
Time: \$60 ALC

LCFC

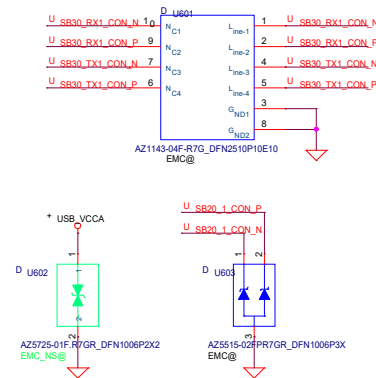


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USB3.0 PORT



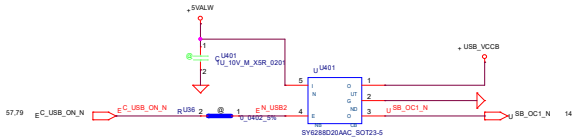
EMC close to USB Conn



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				USB3.0 Port	3
				Date	Sheet 57 of 110

USB2.0 Port and CMC&TVS&CAP MOVE to SUB Board

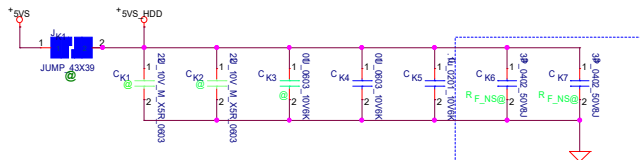
USB2.0 PORT



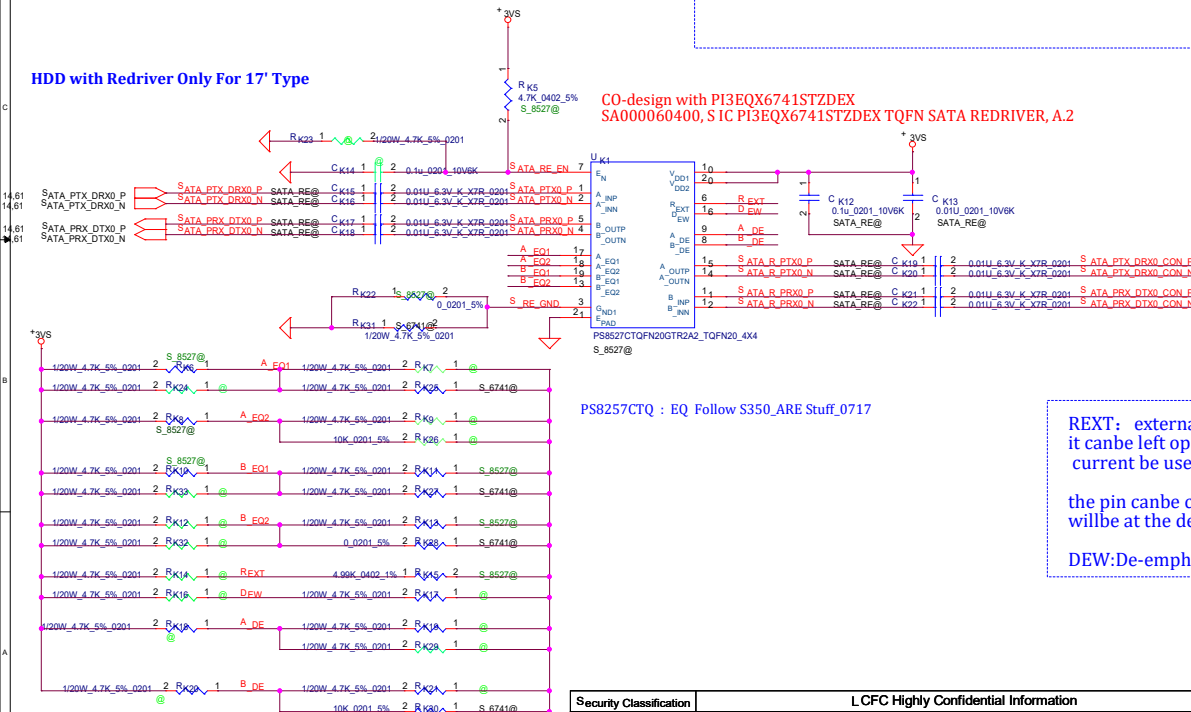
Low Active 2A

the different with Base:
1.S540 No USB2.0 only,S360&V14V15 have

HDD Power



HDD with Redriver Only For 17' Type



CO-design with PI3EQX6741STZDEX
SA000060400, S IC PI3EQX6741STZDEX TQFN SATA REDRIVER, A.2

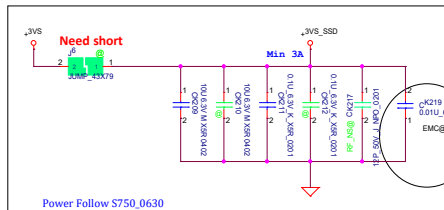
PS8257CTQ : EQ Follow S350 ARE Stuff 0717

REXT: external res for output swing adjustment
it can be left open or tie to GND, internally generated bias
current can be used and the output is as default swing setting;

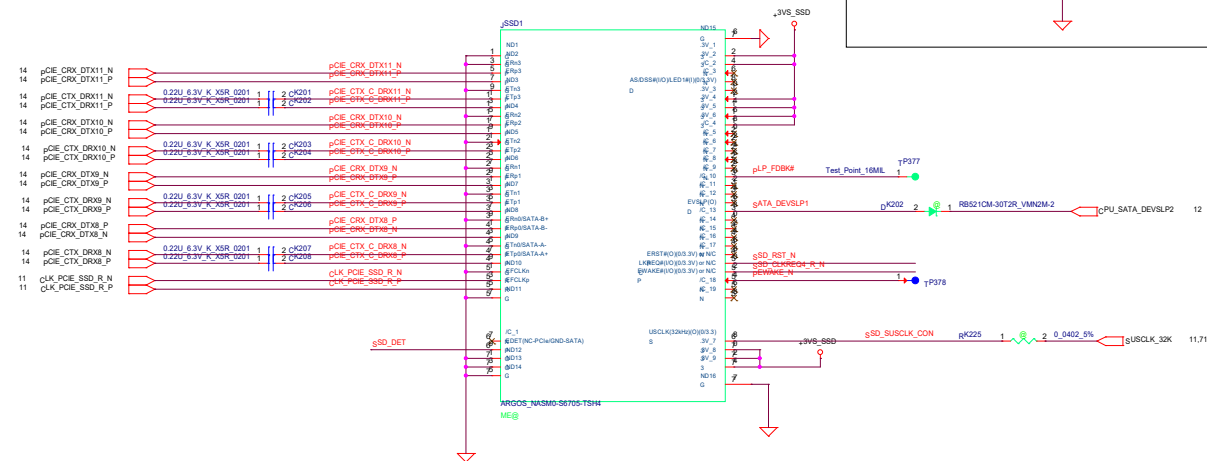
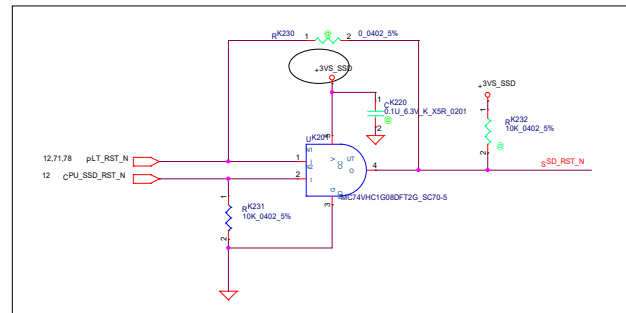
the pin can be connected 4.99k to GND, the output swing will be at the default value with Reference to the ex RES

DEW:De-emphasis width setting for A&B

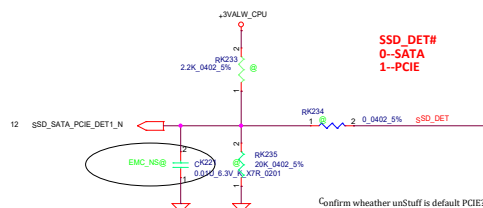
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Issued Date		2012/07/01		Deciphered Date		2014/07/01	
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				HDD		3	
Date				Sheet		61 of 110	
Friday, December 04, 2020							



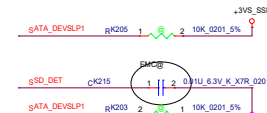
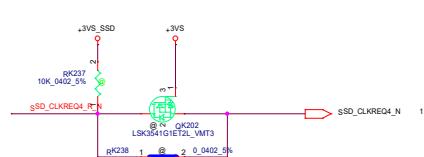
Change CK219 unstuff to 0.01F stuff SVT EMC Require, 20201203



Change CK215 0.1uF unstuff to 0.01F stuff SVT EMC Require, 20201203

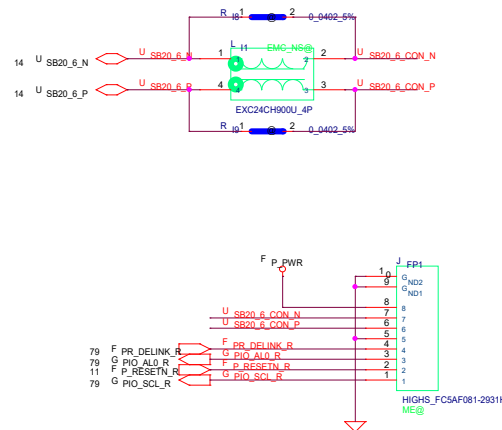
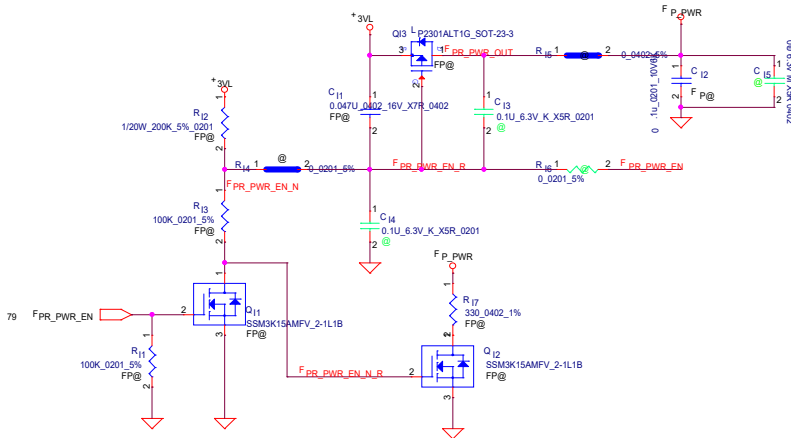


Confirm whether unstuff is default PCIe7

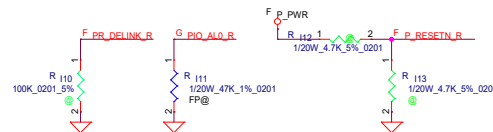
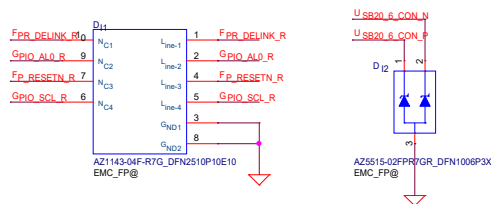


FP Power Control

FingerPrint USB2.0==>APU USB2.0_6



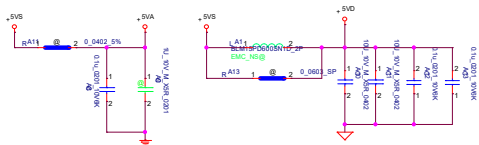
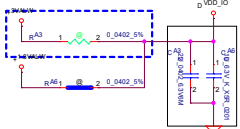
EMC close to Conn



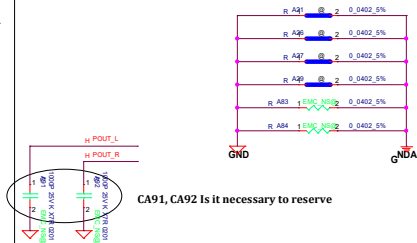
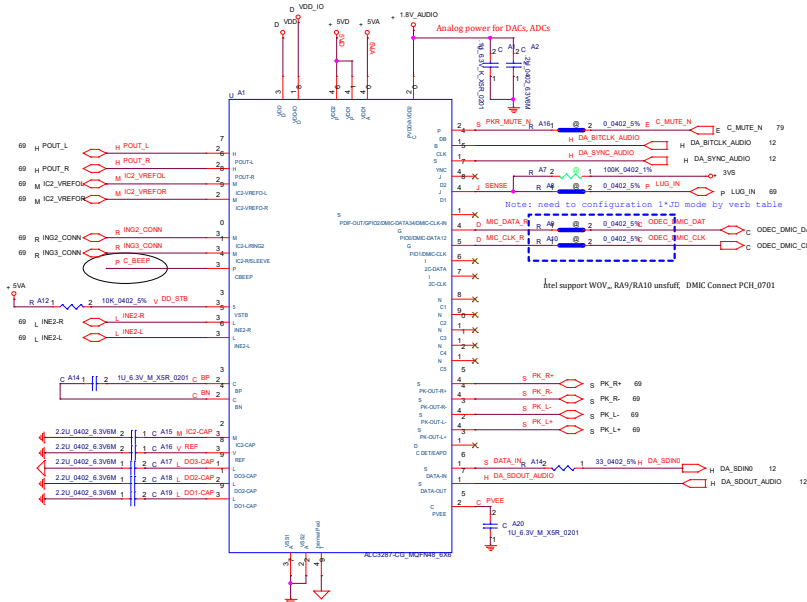
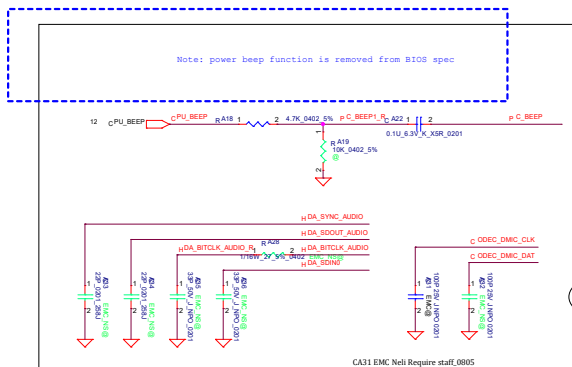
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S360		Document Number		FPR		Revision		3	
Date		December 04, 2020		FPR		Revision		3	
Sheet		6		5		9		110	

the different with Base MODULE:
 1.Module no ra3 to DVDD_IO,S360&V14&V15 reserve
 2.Module no ra5 CA21 to EC_BEEP,S360&V14&V15 reserve

Note: DVDD-IO must be equal to or smaller than DVDD



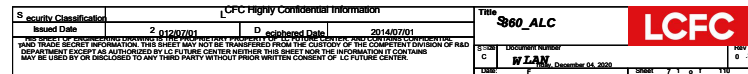
Follow Intel, beep need to confirm_0701




S360_AUC
Card reader Circuit MOVE to SUB Board S360
USB2.0 on SUB Board

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				Card Reader	
				PAGE 0	

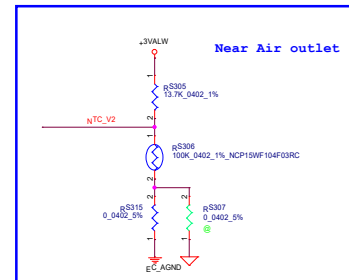
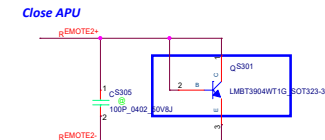
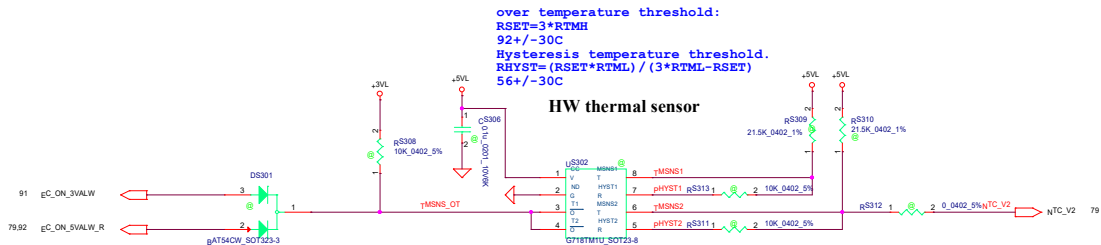
Copy Wlan common design



LAN Circuit MOVE to SUB Board in V360 DB V14V15

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				A		LAN Chipset		0.3	
Date:				Friday, December 04, 2020		Sheet		73 of 110	

FAN Follow Intel 0701



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			USC	SENSOR December 04, 2020	Sheet 77 of 110

USB2.0_1 For USB2.0 Connector;
USB2.0_6 For S360 Card Reader

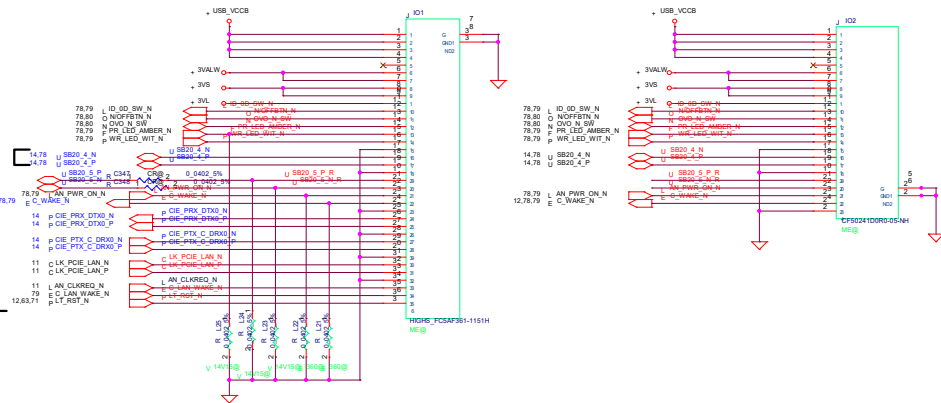
AMD Record USB2.0_4 For USB2.0 Connector;
USB2.0_5 For S360 Card Reader

^PIN23 Intel is PCH_LAN_WAKE_N
AMD IO Board Reservd OR to this PIN:EC_WAKE_N(EC&APU)_0708

EC_LAN_WAKE_N: Lan to EC GPJ7 For V360

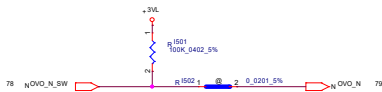
V14V15: USB2.0 LAN

S360: USB2.0 C&R



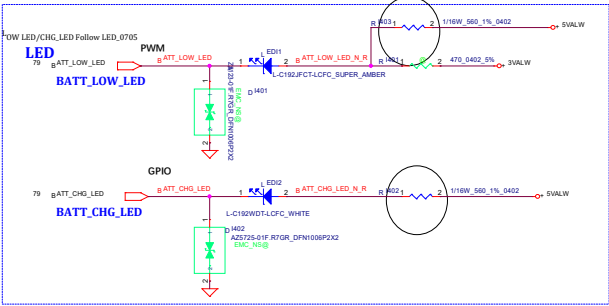
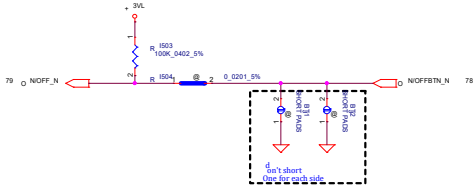


NOVO BUTTON



PWR BUTTON

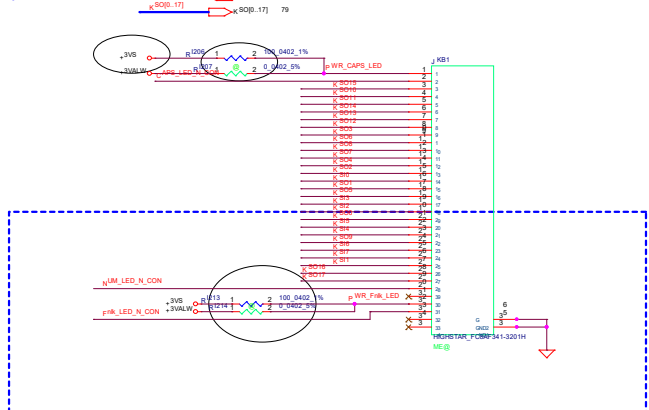
Novo button: follow S750 R1504 OR, Intel 2.2k



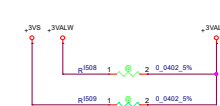
Power LED
check S750_ARH IO Board_0705

LED Behavior	
State	LED Behavior
State (Same as the power button LED)	System on White on (battery 21V-100V)
	Standby LED closed 100ms on, 100ms off (battery 0V-20V)
	System off OFF
Charging	Battery only OFF
	Charging Amber on (battery 1V-90V)
	White on (battery 91V-100V)

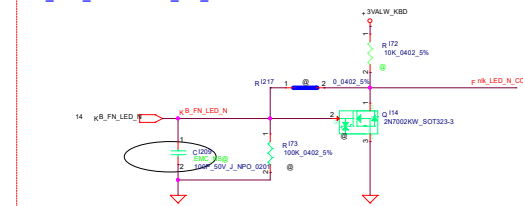
K/B Connector



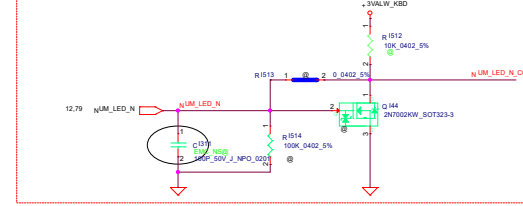
K/B Connector



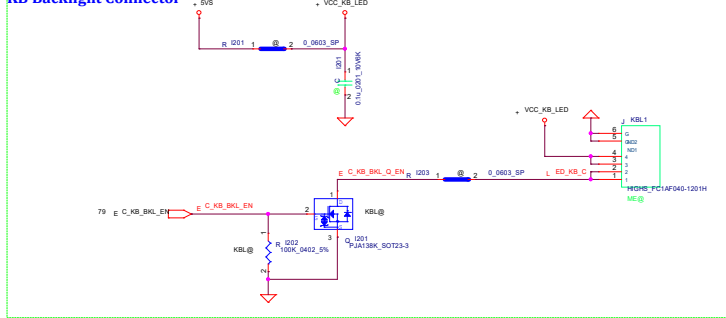
Fnk_LED#_Follow S550_are_0706



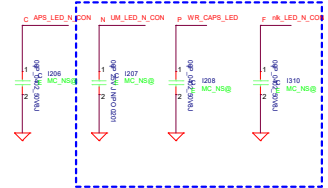
ADD Number LED



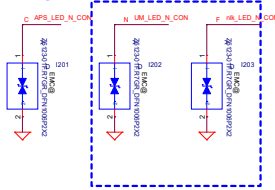
KB Backlight Connector



the diffrent with module:
1.module No 15 KB,S360&V14V15 have



close to Conn
EMC



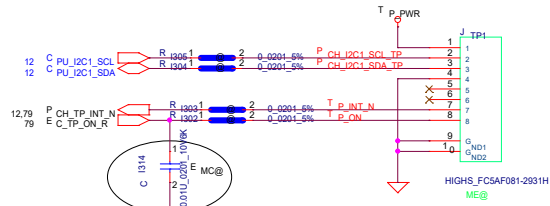
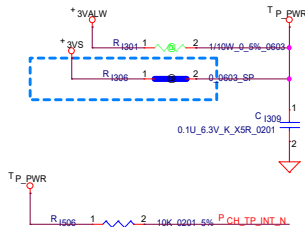
CI209/CI313/CI311 unstuff_ST1003

Touch Pad

(the diffrent with Base MODULE:

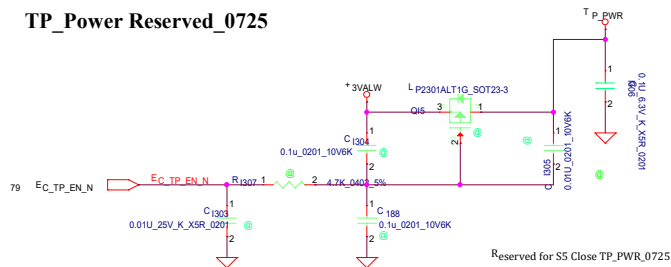
1.Module no RI306,S360&V14&V15 Rerserve) Intel 备注

Need support wake up by touch pad
Follow latest UE spec



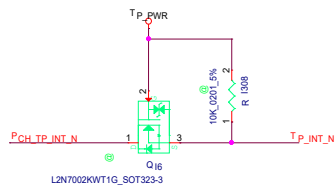
ADD CK314 SVT EMC Require_20201203

TP_Power Reserved_0725



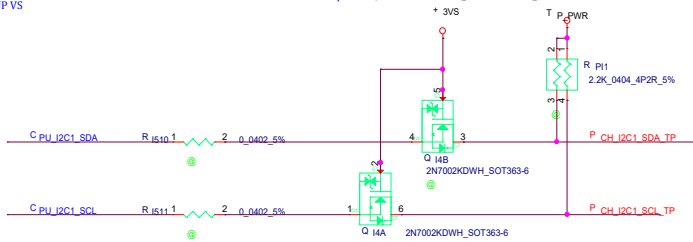
Reserved for S5 Close TP_PWR_0725

Follow S750_ARH ,S750_ARH APU USE S5 Power, S0 Reserve Mosfet 0708



AUP VS

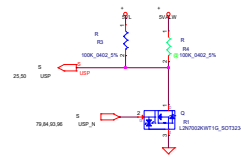
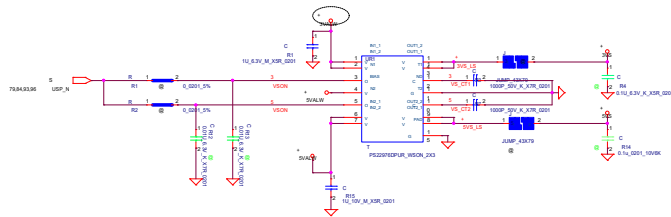
TP If use +3VALW power, need to levelshift, need to check_0702



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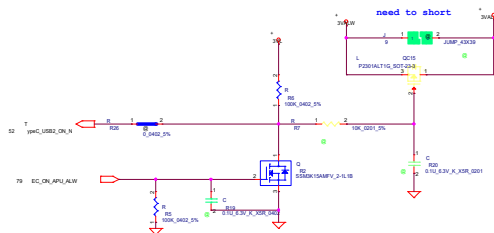
Title		Rev	
S360_ALC		0_3	
S360_ALC		TouchPad_CONN	
Date		Sheet	

3VS/5VS

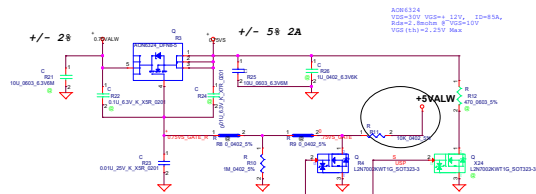


R1 change 2N7002 footprint SOT363-6 to sot323-3

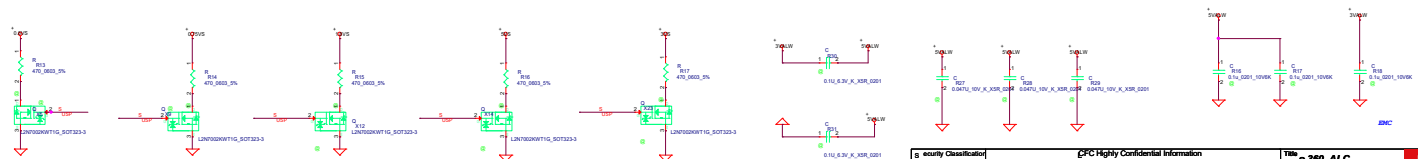
TO +3VALW_APU



TO +0.75VS



For DisCharge



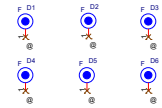
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Page		1		Page		1		Page	
Page		1		Page		1		Page	
Page		1		Page		1		Page	

CPU

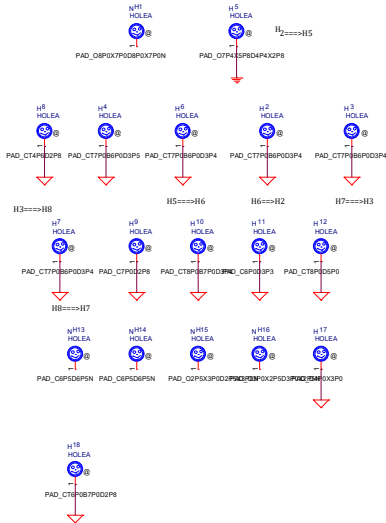
GPU

Memory Shielding

PCB Federal Mark PAD

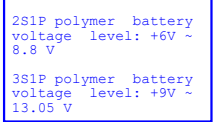


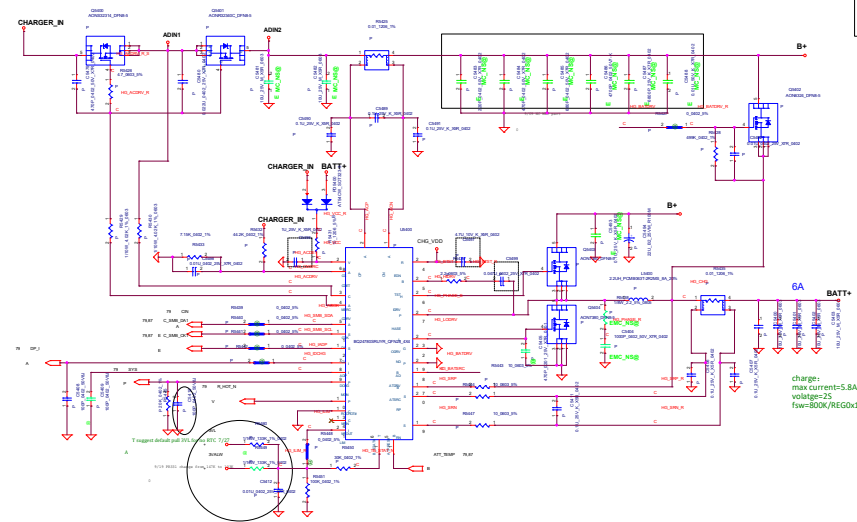
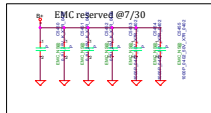
Hole



Shielding







ACDECT setting 17.2V
 Charge current limit HW=7A
 DC discharge limit =28A
 Discharge current limit HW=9A during Turbo boost

charge:
 max current=5.8A
 voltage=25
 fsw=800K/REG0x12[9:8] = 01

IDPM	V(ILIM)	PR5320
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.5A	2.3V	162K
4.0A	2.6V	162K

← LOGIC

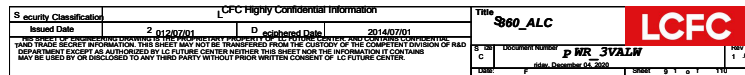
$$V(LIM)=1V+40x(VACT-VCR)=+40xIDPMxRAC$$

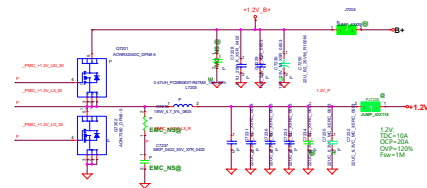
IND IN USE	PR5333
1uH	93K
2.2uH	137K
3.3uH	169K

← LOGIC

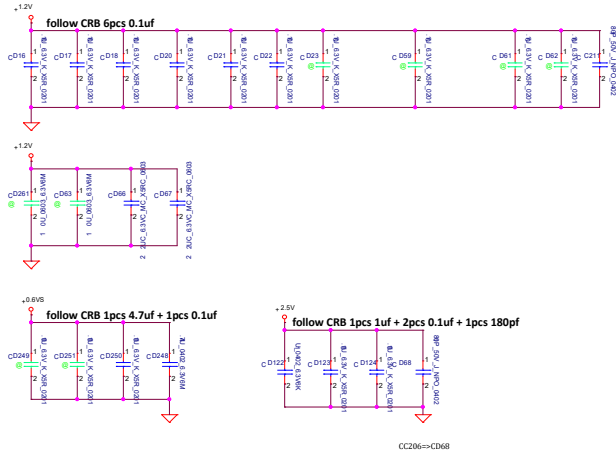
# of CELL	VCELL_PRE	PR5322
1-CELL	1.5V	301K
2-CELL	2.4V	150K
3-CELL	3.3V	82K
4-CELL	4.5V	33.2K

← LOGIC

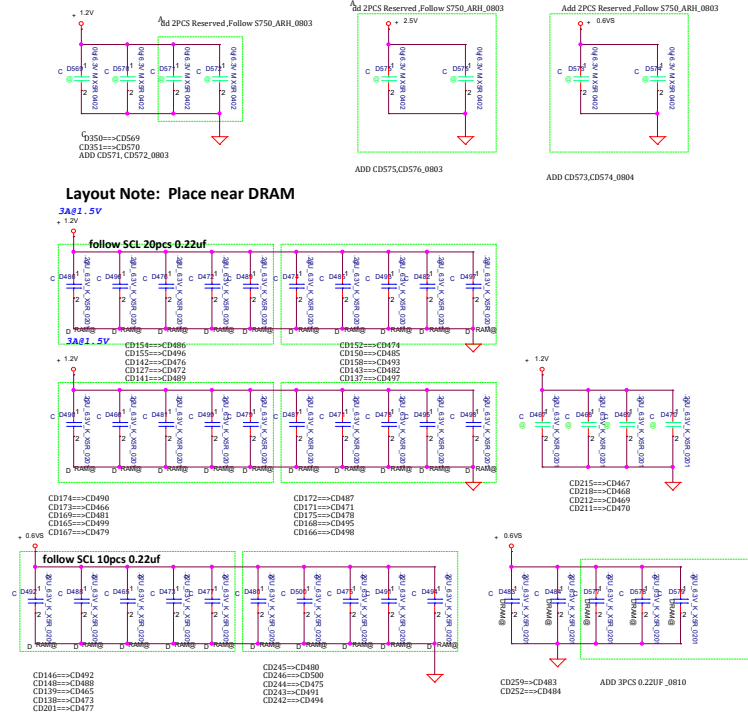


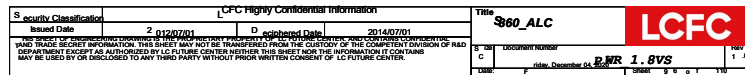


EE Side Channel A SODIMM
Follow S350_ARE_0803

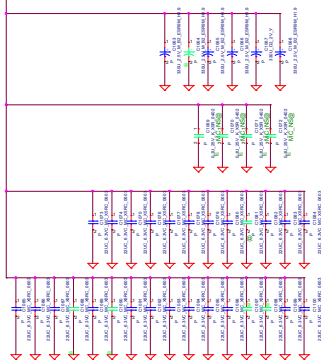


EE Side Channel B MD

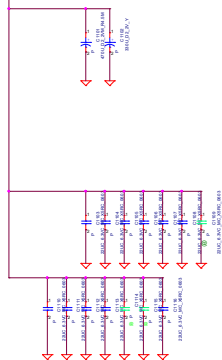




+VDDCR_CPU



+VDDCR_SOC



LCFC Confidential

HS561(NS-D522) IO Schematics Document

Card Reader +hall sensor+FPLED+Button

2020-09

REV: 0.2

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				1	0.2
				Cover Page	
				Monday, September 21, 2020	
				Sheet 1 of 11	

Virtual Symbol_EE

PCB



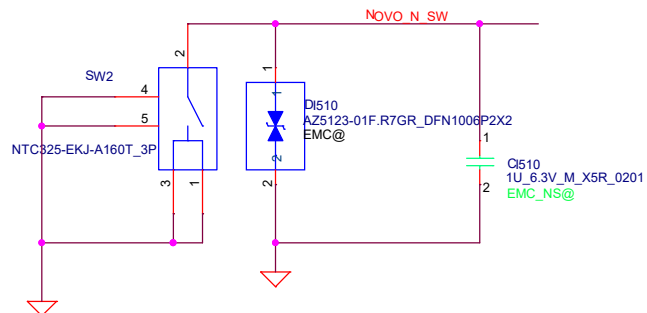
PCB 21P NS-D522 REV0 IO/B
DA600018Q0S

BOM Structure

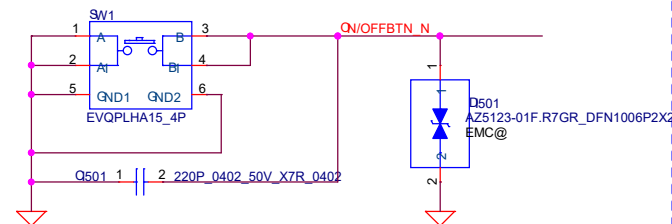
[illegible]

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Date:				Monday, September 21, 2020	Sheet 2 of 11	

Novo switch



ON/OFF switch



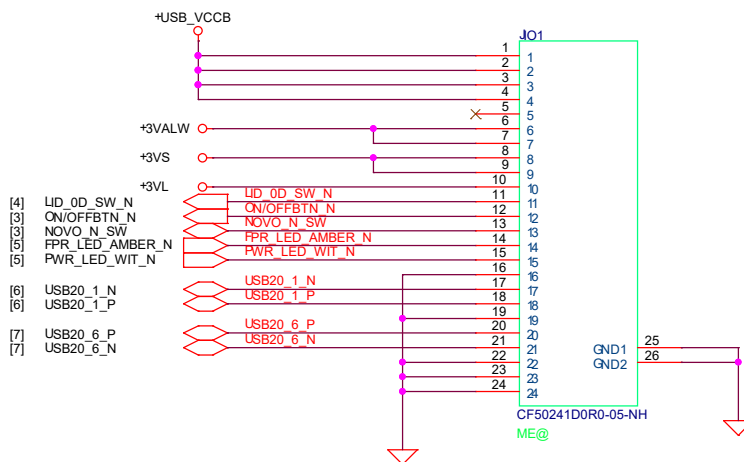
IO CONN



USB2.0 P4

USB2.0
CR

USB2.0 P5



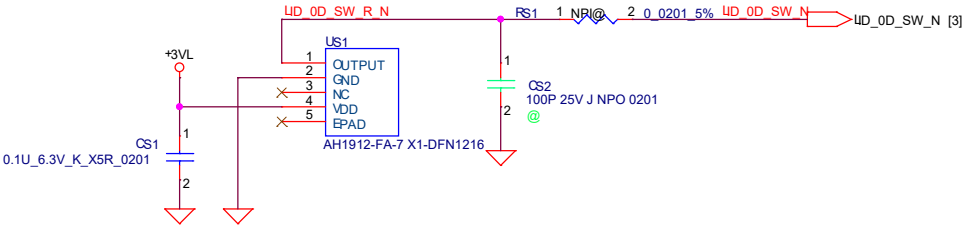
FOR S360 Plastic

USB2.0
Novo BTN
PWR LED
FPR AMBER&WHITE LED
HALL Sensor
SD card

1415 17 IO Common ,connector list type confirm OK,
PIN1 location ok,but wait the layout brd finna confirm.0610
SP010024L0G CF50241D0R0-05-NH

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				IO CON/Power Button	
				Date:	Monday, September 21, 2020
				Sheet	3 of 11
				Rev	02

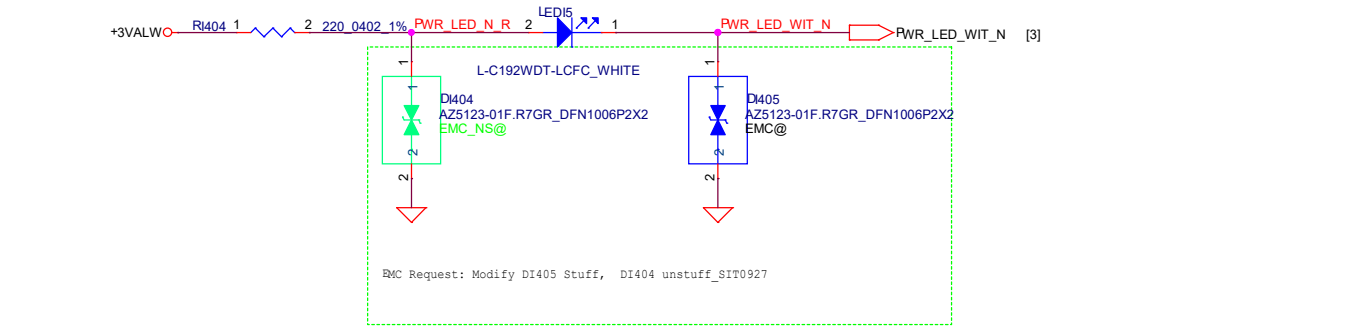
LID switch



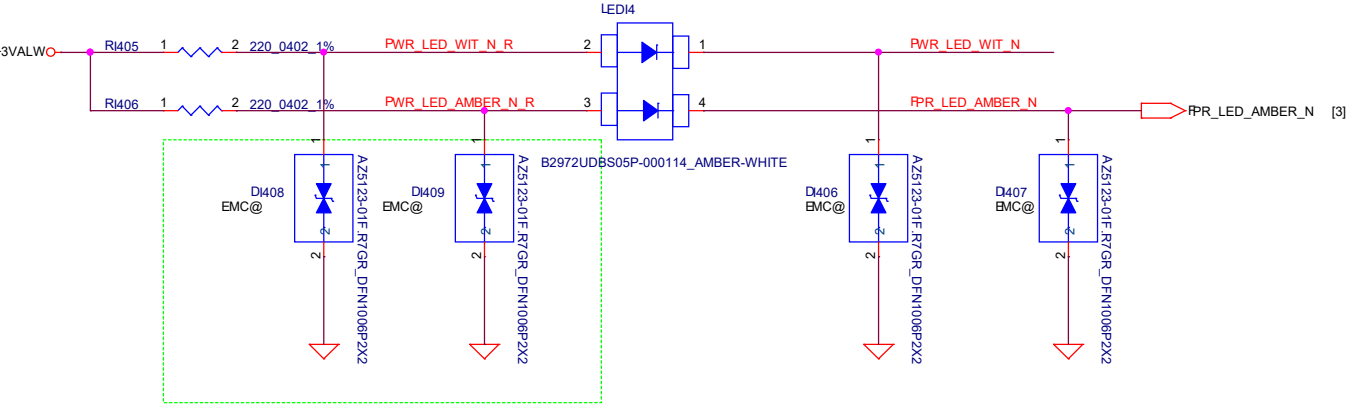
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Title		S 360-ALC-IO DB	LCFC
Size	Document Number		
B	Hall sensor	Rev	02
Date:	Monday, September 21, 2020	Sheet	4 of 11

POWER_LED LENSE

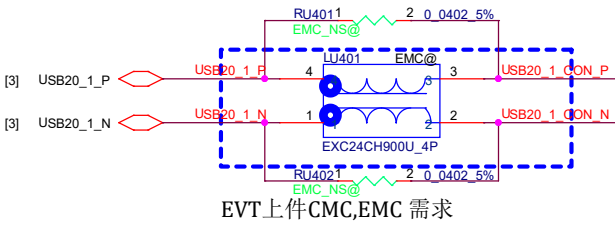


FP_LED

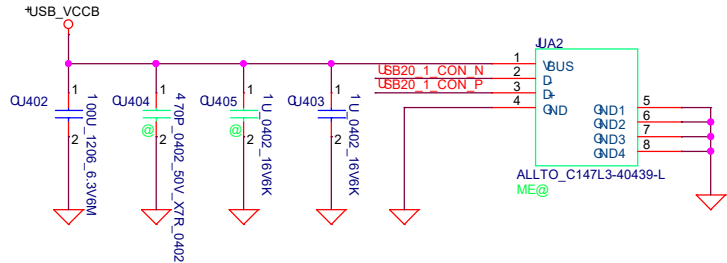
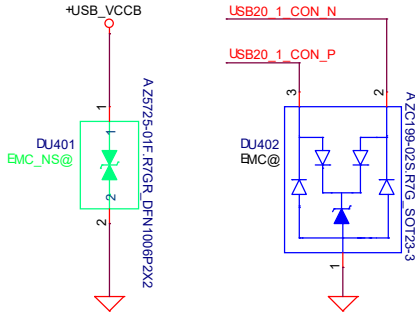


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Size B		Document Number FP LED				Rev 12			
Date:		Sunday, September 27, 2020				Sheet		5 of 11	

USB2.0 CONN
APU Port 4
Power Switch place In The MB

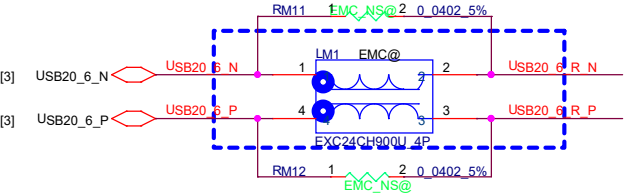


For ESD
close to USB Conn

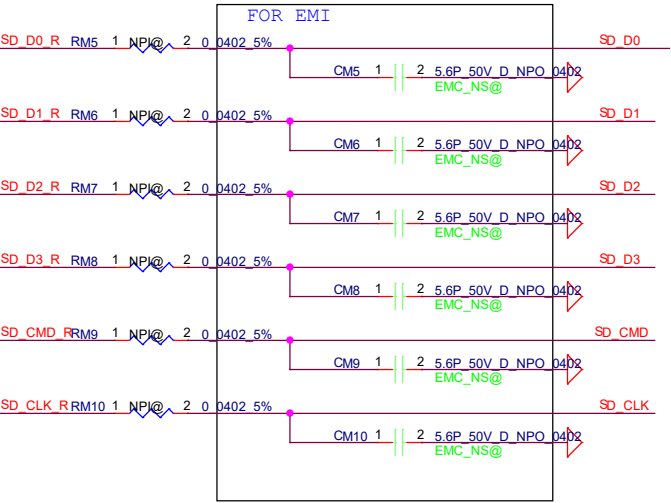
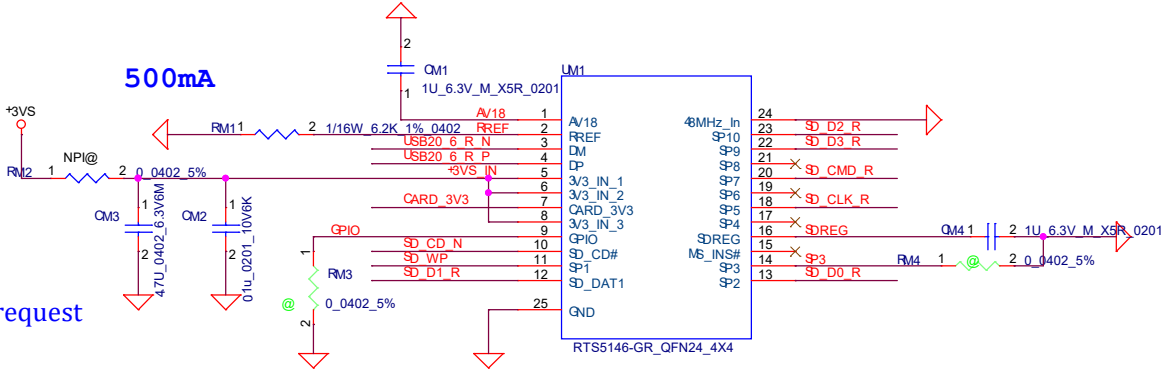


1415 17 IO Common ,connector list type confirm OK,
ALLTOP DC23300HW00 C147L3-40439-L
.0610

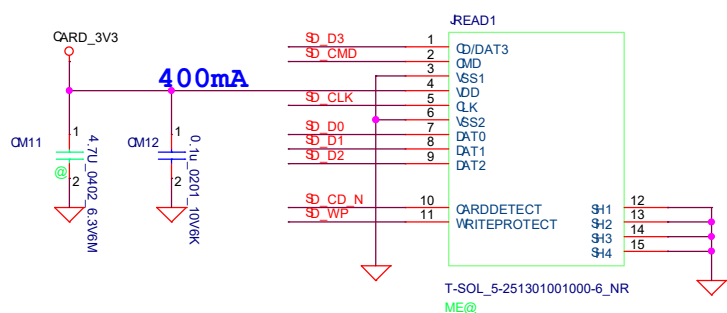
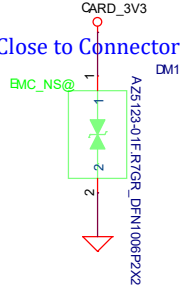
Card Reader
APU Port 5



Diffrence with Common design module:EVT Stuff CMC,EMC request

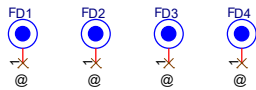


Close to Connector

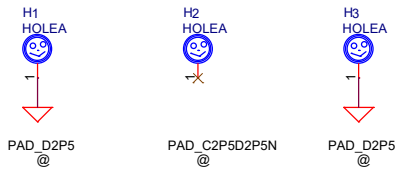


1415 17 IO Common ,connector list type confirm OK,
TAISOL SP07000WG00 5-251301001000-6
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PCB Fedcal Mark PAD



Hole



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